

Trap-related frequency dispersion of zero-bias microwave responsivity at low temperature in GaN-based self-switching diodes

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Abstract

The zero-bias microwave detection capability of self-switching diodes (SSDs) based on AlGaIn/GaN is analyzed in a wide temperature range, from 10 K to 300 K. The measured responsivity shows an anomalous enhancement at low temperature, while the detected voltage exhibits a roll-off in frequency, which can be attributed to the presence of surface and bulk traps. To gain a deep insight into this behavior, a systematic DC and AC characterization of the diodes has been carried out in the mentioned temperature range. DC results confirm the existence of traps and AC measurements allow us to identify their properties. In particular, impedance studies enable to distinguish two types of traps: at the lateral surfaces of the channel, with a wide spread of relaxation times, and in the bulk.

Keywords: Self-switching diode, GaN, trapping effects, impedance measurements, microwave detection

(Some figures may appear in colour only in the online journal)

1. Introduction

In recent years, to cover the unceasing needs for high frequency and high power technology, significant attention has been focused in nitride-based semiconductors, specially Gallium Nitride (GaN). The main advantages of GaN are its wide bandgap, high thermal conductivity, low relative permittivity, high breakdown electric field, high thermal stability, moderately high electron mobility and high saturation velocity [1–3]. Moreover, devices based on the AlGaIn/GaN heterostructure are hugely interesting owing to the high carrier concentration achieved in the two-dimensional electron gas (2DEG) [4]. Numerous efforts have been invested to make the AlGaIn/GaN devices run smoothly at high power and high

frequency, including the improvement of the material quality in epitaxial and passivation layers, the selection of the suitable substrate and the optimization the AlGaIn barrier thickness [5, 6]. In spite of the enhancements achieved, current devices still have limitations in their microwave performance due to the presence of traps located at the surfaces (either on the top of the AlGaIn layer or at the sidewalls of etched regions) [7] or in the bulk of GaN (being usually caused by lattice defects such as vacancies, dislocations, etc) [8–11]. Surface traps found at the top of the AlGaIn layer contribute to deplete the 2DEG near the interface with GaN and therefore degrade the dynamic device performance [12]. In the case of nanochannels or Fin-FETs, the damage caused by etching processes can also originate the presence of numerous

intermediate surface states distributed within the gap that may laterally deplete the channel and also affect the dynamic performance, being especially critical in narrow regions [13]. Finally, electrons captured by traps in the bulk may also deplete the 2DEG, causing a rise of the resistance and a reduction of the drain current. These trapping mechanisms present in GaN devices result in frequency dispersion phenomena in their electrical characteristics, thus limiting RF applications. Many characterization methods, such as low-frequency noise measurements, electron tunneling spectroscopy (ETS) [14], deep-level transient spectroscopy (DLTS) [15], quantitative mobility spectrum analysis (QMSA) [16] and impedance measurements [17], are customarily used to study the trapping mechanisms.

In this work we deal with devices potentially affected by several of the above mentioned traps, Self-Switching Diodes (SSDs) fabricated on an AlGaIn/GaN heterostructure grown on a Si substrate. The SSD, proposed by A M Song in 2003 [18], is an asymmetric planar nanodiode with a conductive nanochannel defined by the etching of two L-shaped insulating trenches, whose asymmetry produces a non-linear current-voltage relationship which, in turn, allows to detect millimeter-wave signals at zero-bias [19]. The breaking of the channel symmetry provides a rectifying behaviour without the use of any doping junction [20]. Due to the high surface-to-volume ratio of SSDs, one of the main issues is the presence of surface states originated by the etching process, causing the shrinking of the effective channel width [18] and limiting their reliability [7]. Despite the above mentioned concerns, the good SSD performance as THz detector has been proved for different materials, such as InAs [19], GaAs [21] and InGaAs [22], including the optimization through channel geometrical parameters, width and length, and the number of channels in parallel [23]. Concerning GaN-based SSDs, even if not showing an evident rectifying behaviour as showed by narrow InGaAs or GaAs SSDs [18, 21, 22], they have demonstrated their validity as RF detectors, exhibiting a responsivity up to 100 V W^{-1} at 0.30 THz [24] and 2 V W^{-1} (in free-space) at 0.69 THz [25]. Indeed, recently, more complex structures have been studied, such as Gated-SSDs (GSSDs), which are SSDs with a Schottky gate [26], or gated nanowire field-effect rectifiers (NW-FERs) [27], with responsivities of 600 V W^{-1} and 3000 V W^{-1} , respectively.

The objective of this paper is to analyze the impact of temperature on the microwave detection capabilities of GaN SSDs, in particular on the responsivity, which exhibits an unexpected behavior that we attribute to the presence of traps, also reflected in the DC I - V curves. Impedance measurements, proved to be a powerful tool to identify trapping effects [9, 10, 17, 28], are employed to get more insight into the properties of the traps present in SSDs. The results evidence the presence of both bulk and surface traps, the latter involving a spread of relaxation times [29, 30], consistent with the presence of lateral surface states at both sides of the channel.

The paper is organized as follows. In section 2, we describe the devices under test and the different experimental setups. In section 3, first the results of RF characterization are shown, then the measured DC I - V curves are analyzed to corroborate

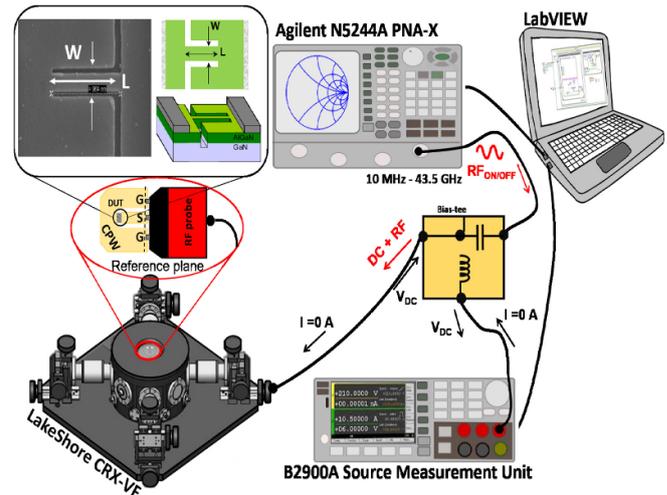


Figure 1. Experimental setup for RF detection. A cryogenic probe station connects the device to a vector network analyzer, operating simply as the RF power supplier, and to a source measurement unit, which allows to bias at zero-current and records the output voltage. The bias-tee is actually inside the PNA-X.

the RF operation by means of a quasi-static model and, finally, impedance measurements are used to interpret the previous results in terms of the presence of traps and to identify their characteristics. At last, the main conclusions are drawn in section 4.

2. Device under test and setup

The SSDs under test were fabricated on an AlGaIn/GaN heterojunction grown by EpiGaIn by means of metal oxide chemical vapor deposition (MOCVD) on a high resistivity Si substrate. The epitaxial stack consists of 25 nm of $\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}$ and $1.5 \mu\text{m}$ of GaN on a Si substrate (thickness $575 \mu\text{m}$) and passivated with 3 nm of SiN. The asymmetric shape of the channel was defined using dry etching [24]. Initially, we focus our attention on a device consisting in a single channel, $L = 1 \mu\text{m}$ long and $W = 80 \text{ nm}$ wide. Measurements were done on-wafer at temperatures ranging from 10 K to 300 K.

The setup used for the on-wafer characterization of the device is modified depending on the kind of measurements and, thus, diverse equipments are chosen. For all configurations, the wafer is inside a cryogenic probe station (LakeShore CRX-VF), where a controller stabilizes the temperature (10 K–300 K). Depending on the type of measurement, RF or DC probes are used to contact the accesses of the SSDs. The setups are controlled by means of a dedicated home-made LabVIEW code.

For the first kind of on-wafer characterization, RF measurements to determine the responsivity of the devices, the setup shown in figure 1 has been used. The RF power is injected with a vector network analyzer (Agilent N52 444A PNA-X) in the frequency band between 100 MHz and 40 GHz by means of $100 \mu\text{m}$ pitch RF probes in a Ground-Signal-Ground (GSG) configuration. For this sake, in the fabrication process, CPW accesses with a $30 \mu\text{m}$ signal line and a $20 \mu\text{m}$ spacing in order

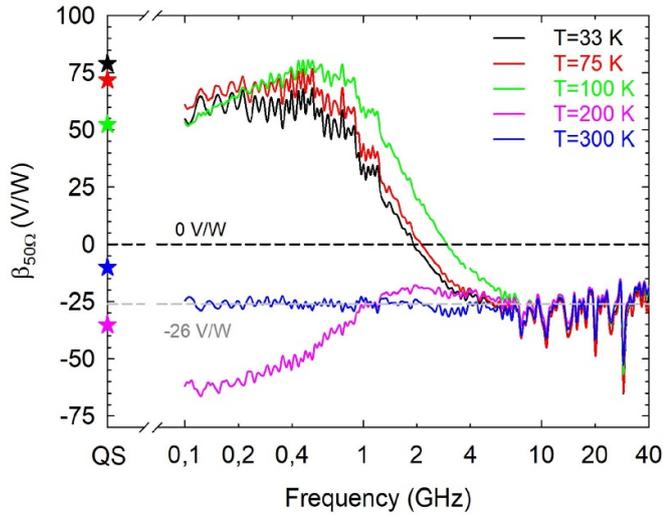


Figure 2. Responsivity, $\beta_{50\Omega}$, at zero bias as a function of frequency between 100 MHz and 40 GHz with a -5 dBm input power. The stars correspond to the values obtained with the quasi-static (QS) model.

to provide a $50\ \Omega$ characteristic impedance are coupled to the SSDs. A bias-tee and a Keysight B2900A Source Measurement Unit (SMU) were employed to bias the diode with zero current and record the measured output voltage. Furthermore, to estimate the power delivered to the SSD at the reference plane (P_{in}), the losses due to the cables, connectors and probes were taken into account at each frequency and each temperature. More details of the setup can be found in [31]. In the DC regime, just the mentioned SMU was used to measure the I - V curves. Finally, the equipment to measure the impedance dependence on the frequency was an Agilent 4285A precision LCR meter (75 kHz–30 MHz), which applies a small sinusoidal signal of $30\ \text{mV}_{rms}$ to the device.

3. Results and discussion

3.1. RF measurements

Figure 2 shows the results of the zero-bias RF characterization in the temperature range from 10 K up to 300 K. Responsivity is easily computed as

$$\beta_{50\Omega} = \frac{\Delta V}{P_{in}}, \quad (1)$$

where P_{in} is the value of the RF input power at the reference plane (-5 dBm, with losses already compensated by increasing the VNA output power) injected by a $50\ \Omega$ source and ΔV is determined as the difference between the DC voltage generated by the SSD with and without RF signal (figure 1). An anomalous behaviour is observed not only in temperature but also in frequency: a remarkable enhancement of responsivity is found when lowering T for frequencies below 1 GHz, and its sign changes around 150 K. In addition, concerning the frequency behaviour, at room temperature $\beta_{50\Omega}$ shows a flat

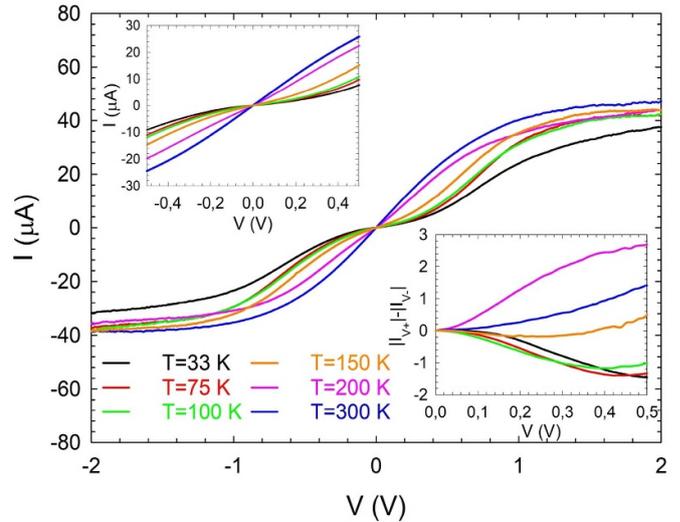


Figure 3. I - V curves of the SSD under test (80 nm width and $1\ \mu\text{m}$ length). The top left inset shows a zoom of 500 mV around zero bias. The bottom right inset displays the current difference between positive and negative voltage around zero bias.

behaviour, taking a value about $-26\ \text{V W}^{-1}$, while for lower temperatures a roll-off is present around 1 GHz, to finally reach the same constant value than for 300 K. These results evidence the presence of a phenomenon at low temperature and low frequency, which vanishes at higher temperatures (> 200 K). In order to understand these findings and check if they are also present in the static response of the device, the DC behavior of the SSD is analyzed in next sub-section.

3.2. DC measurements

It is well-known that the non-linearity of the I - V curve is closely related to square-law detection of small signals [32]. To identify such non-linearity, a DC measurement in a voltage range from $-2\ \text{V}$ to $2\ \text{V}$ within the same temperature range was performed. Figure 3 shows the measured I - V curve at different temperatures, where an unusual behavior is observed again. While an increase of drain current was expected at the lowest temperatures due to a higher mobility, surprisingly, a decrease of the current at low bias is revealed for the lowest values of T . A good quality of the ohmic contacts has been confirmed, and so we attribute this behavior to the increase of the depletion region caused by electrons trapped at surface states present at the sidewalls of the trenches defining the channel, originated by the etching process [7]. Figure 3 suggests that the surface depletion has a strong impact at low temperatures, becoming less influential when electrons are released from the traps at increasing T . To determine the width of the depletion region at room temperature, an analysis for different channel widths was carried out [13], finding that the depletion region is about 25 nm at each side of channel, similar to that found in SSDs with identical structure [31]. If at lower temperatures more electrons are trapped at the surface states, it is expected that the channel is nearly completely closed, as observed in the top inset of figure 3. This observation is accompanied

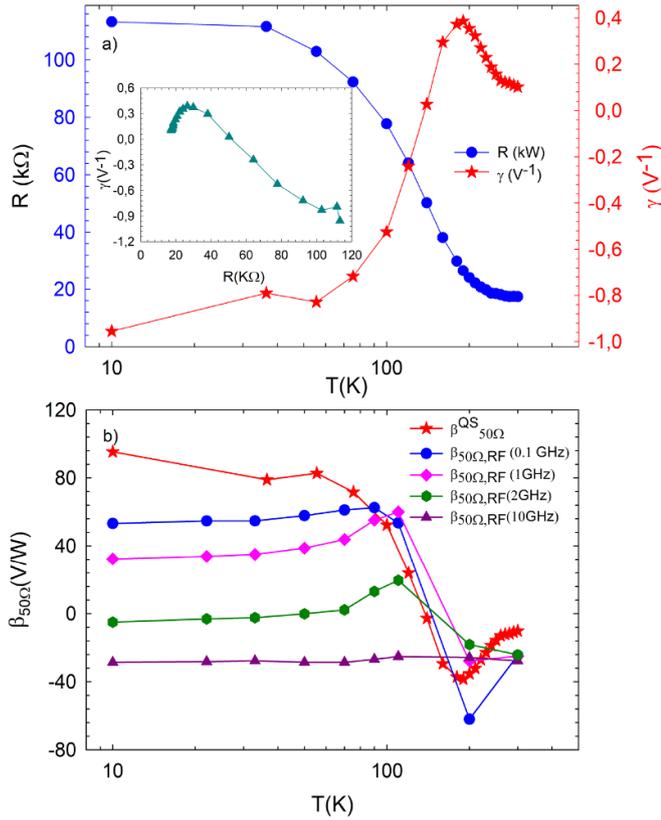


Figure 4. (a) Resistance, R , and bowing coefficient, γ , obtained with the QS model as a function of T (the inset shows γ vs R). (b) Responsivity obtained with the QS model, $\beta_{50\Omega}^{QS}$, and measured responsivity, $\beta_{50\Omega}$, at different frequencies (0.1 GHz, 1 GHz, 2 GHz and 10 GHz), as a function of T .

by a revealing change in the curvature sign at low bias around 150 K, as well as in the asymmetry of the I - V curve; see the bottom inset of figure 3, where the current difference between positive and negative bias is plotted, being negative for $T < 150$ K, positive for $T > 150$ K and almost zero for $T = 150$ K.

In order to link the RF results with the DC measurements, a simple quasi-static (QS) model, proposed in [33], is applied, allowing to estimate the responsivity at low-frequency through the coefficients obtained from the Taylor series expansion of the I - V curve. By means of a polynomial fitting around equilibrium of each of the I - V curves (500 mV, see top left inset of figure 3), it is straightforward to obtain the differential resistance, $R = \frac{\partial V}{\partial I}$, and the bowing coefficient, $\gamma = R \frac{\partial^2 I}{\partial V^2}$, the results are shown in figure 4. The low-frequency QS responsivity is then obtained as:

$$\beta_{50\Omega}^{QS} = -\frac{1}{2} R \gamma (1 - \Gamma^2), \quad (2)$$

$\Gamma = \frac{R - Z_0}{R + Z_0}$ being the reflection coefficient, required to compute the reflected power due to the mismatch between the nanodiode (R) and the transmission line ($Z_0 = 50 \Omega$). In figure 4(a), a monotonous increase of R is observed when the temperature is lowered, but a more complex pattern is present in γ . As T decreases from room temperature, γ initially grows, reaching a maximum at $T \approx 200$ K, changing sign at $T \approx 150$ K and then

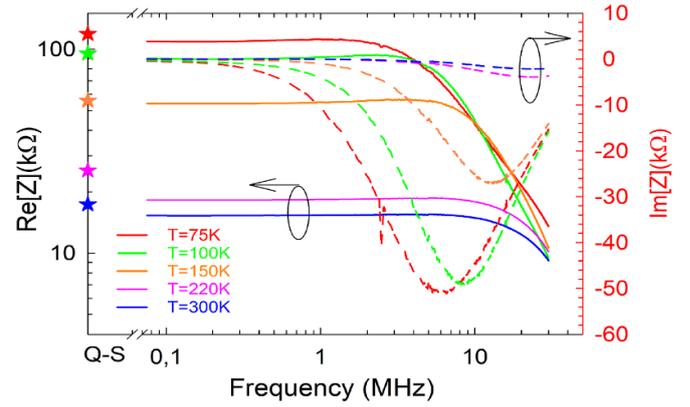


Figure 5. Real ($\text{Re}[Z]$, solid lines, left axis) and imaginary ($\text{Im}[Z]$, dashed lines, right axis) parts of the impedance as a function of frequency measured at different temperatures. The stars represent the zero-bias resistance obtained from DC measurements at the same temperatures.

becoming stable below 100 K. The inset of figure 4(a) shows the relation between γ and R . Finally, in figure 4(b), the low-frequency responsivity exhibits a similar aspect to γ , and, due to the severe mismatch, it is very close to the theoretical value of $2Z_0\gamma$ [31]. For the lowest temperatures, $\beta_{50\Omega}^{QS}$ shows a constant value around 80 V W^{-1} , then changing sign at 150 K and reaching a minimum at $T \approx 200$ K.

Going further, if we compare $\beta_{50\Omega}^{QS}$ with $\beta_{50\Omega}$ measured at different frequencies, see figure 4(b), a reasonably good agreement is achieved in the whole temperature range at the lowest measured frequency (0.1 GHz). The change in sign that occurs approximately at 150 K could be attributed to the presence of some kind of thermally activated traps that affect carrier concentration in the channel, which are also responsible for the anomalous behavior of the DC curve previously discussed. In contrast, $\beta_{50\Omega}$ turns to be practically constant with temperature at high frequency, suggesting that traps only react for frequencies below 2 GHz. In order to clarify the type, location and activation energy of the traps, an impedance analysis was accomplished, as reported in next subsection.

3.3. Impedance measurements

By means of the setup for impedance measurements described in section 2, we extract the real, $\text{Re}[Z]$, and imaginary, $\text{Im}[Z]$, parts of the impedance of the SSDs in order to identify the signature of the traps present in the diodes. The results are shown in figure 5 in the range 75 kHz–30 MHz (determined by the available equipment). Temperatures from 75 to 300 K have been studied. The stars in the figure correspond to the QS resistance of figure 4(a) and show the expected good agreement with the low-frequency value of $\text{Re}[Z]$ at each temperature. For all temperatures, an initial plateau followed by a drop-off is found in $\text{Re}[Z]$ as a function of frequency. On the one hand, in the plateau, the lower the temperature the higher the value of $\text{Re}[Z]$, suggesting that traps, either in surface or bulk, respond by capturing 2DEG electrons, causing a decrease of the electron density in the channel and thus leading to an

increase of resistance. On the other hand, for the highest temperatures in the studied range, once most of the electrons have been released by the thermal activation of the traps, $\text{Re}[Z]$ exhibits a weaker frequency and temperature dependence [28]. In the high-frequency region ($f > 10$ MHz), traps no longer respond to the signal, causing the drop-off of $\text{Re}[Z]$, which, remarkably, takes place at a higher frequency as temperature increases.

$\text{Im}[Z]$ also shows a characteristic behavior. A clear minimum that shifts towards higher frequency and decreases in amplitude with the increase of temperature is observed, again confirming the presence of a phenomenon whose influence is smaller as temperature is raised. It is worth noticing that the minimum of $\text{Im}[Z]$ and the drop-off of $\text{Re}[Z]$ match in frequency, indicating that traps affect both parts of impedance and stop responding beyond the frequencies. The frequency at which the peak takes place in $\text{Im}[Z]$ (coincident with the drop-off of $\text{Re}[Z]$) allows identifying a characteristic time for the relaxation process at each temperature, $\tau_{peak} = 1/f_{peak}$.

By inspection of the impedance, it seems that, due to the thermal activation, trapping effects become less significant for $T > 200$ K, but they do not completely disappear. To identify the origin of the traps (type, location) and confirm their presence in other geometries, measurements in wider SSDs, with channel widths of 124 and 150 nm, were also performed as a function of temperature. Measurements exhibit a similar behavior to that observed in figure 5, but with different characteristic frequencies of the minimum in $\text{Im}[Z]$, also coinciding with the drop-off in $\text{Re}[Z]$. We have identified the corresponding characteristic time τ_{peak} and plotted it as a function of temperature in figure 6 for the three diodes under analysis. Two different behaviors (slopes) are observed in the figure, more evident when the width of the SSD increases, indicating the coexistence of two kind of trapping mechanisms. At the lower temperatures, the characteristic time exhibits a decrease that becomes more pronounced (larger slope) at higher temperatures. The initial behavior is the dominant in the narrowest diode (it extends in a larger temperature range), while the second one is more relevant in the wider SSDs.

Bulk traps were identified in AlGaIn/GaN HEMTs through low frequency Y-parameters measurements in [9, 10], which allow obtaining the trap activation energy (E_a) and cross section (σ_n). Interfacial traps were also detected in similar devices as a result of frequency dispersion in capacitance and conductance [17]. As will be shown in the following, the characteristic time found in our measurements at the higher temperatures exhibits a similar temperature dependence to that of bulk traps [9, 10]. However, that is not the case of our results at low temperature, whose behavior fits much better the case of a spread of relaxation times instead of a single one. Impedance measurements have also been used in the literature to identify thermally activated processes where the relaxation times are distributed over a given range. These processes are typically present in materials whose resistance decreases with increasing temperature, and are related to grain boundary effects and the release of space charge [29, 30]. In AlGaIn/GaN devices, there are also phenomena whose lifetimes are expected to

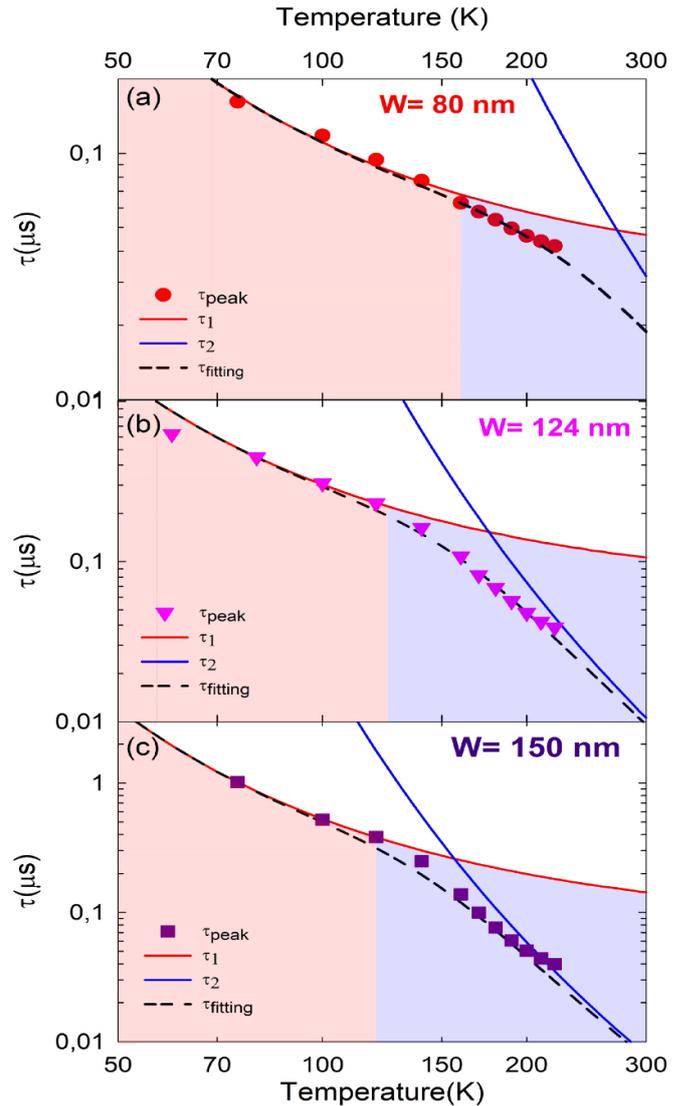


Figure 6. Experimental values of τ_{peak} extracted from the minimum of $\text{Im}[Z]$ at each temperature (symbols) for the SSDs with different channel widths, W : (a) 80 nm, (b) 124 nm and (c) 150 nm. The red and blue lines show the fittings of the times corresponding to surface (τ_1) and bulk (τ_2) traps, respectively, while the dashed line corresponds to the resulting global time computed as $\tau_{fitting} = \frac{\tau_1 \cdot \tau_2}{\tau_1 + \tau_2}$. The red shaded area indicates the temperature range where the behavior is dominated by surface traps and the blue one the range where both traps are influencing.

be spread over a certain range of times at a given temperature [34]. For example, in the case of surface states, capture and emission occurs from a band of states rather than discrete levels [35, 36]. In the SSDs studied here, we have observed a decrease in resistance with the increase of temperature (figure 4(a)), attributed to the release of charge trapped at the surface states present in the sidewalls of the channel. These surface states, originated during the etching process, are distributed in energy inside the semiconductor gap. Therefore, relaxation processes exhibiting a behavior related to a spread of times can be expected in SSDs, specially when they are narrow and the surface-to-volume ratio is very high. Indeed, for the lowest temperatures, the relaxation mechanism, which

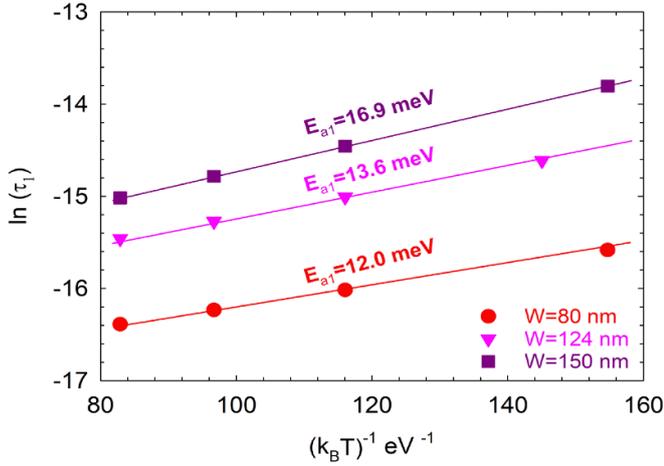


Figure 7. Arrhenius plot for the relaxation times at the lower temperatures ($T < 150$ K) in SSDs with different widths. The symbols correspond to the experimental data and the lines are the fitting of the data to equation (3).

we attribute to intermediate surface states, follows the Arrhenius relation typical from a spread or times characterized by a global activation energy E_{a1} ,

$$\tau_1 = \tau_{01} \cdot \exp\left(\frac{E_{a1}}{k_B T}\right), \quad (3)$$

where τ_{01} is a pre-exponential factor independent of temperature and k_B is the Boltzmann constant. To estimate the effective energy, a fitting of the experimental data to the equation (3) at the lower temperatures ($T < 150$ K) was made, see figure 7. As a result, different effective energies were found, which vary from 12 meV to 17 meV depending of the width of the SSD, what suggests that the location of the intermediate states is similar, but not exactly the same, for each device.

The red lines in figure 6 correspond to the times obtained with this fitting for each diode. In view of the figure, it seems clear that the surface states are dominant for the lower temperatures and their presence is more remarkable in the narrow devices. In particular, if we estimate the temperature corresponding to the global activation energy in the SSD with $W = 80$ nm, 12 meV, a value $T_{a1} \approx 140$ K is obtained as $E_{a1} = k_B T$ just the temperature at which the bowing coefficient (figure 4(a)) and responsivity (figure 2) change their sign.

All of the above effects point to the presence of intermediate surface states which are charged at low temperatures, but they are not enough to explain the SSD performance over the full temperature span and, thus, a second type of trap must be considered. The existence of a second trap, whose influence is more obvious in wider SSD, becomes evident at higher temperatures, where the characteristic time τ_{peak} versus T changes its slope, as discussed before. If we assume that apart from the surface traps characterized by τ_1 , a second kind of traps with a relaxation time τ_2 is present in our devices, at each temperature τ_{peak} should obey

$$\langle \tau_{peak} \rangle^{-1} = \langle \tau_1 \rangle^{-1} + \langle \tau_2 \rangle^{-1}. \quad (4)$$

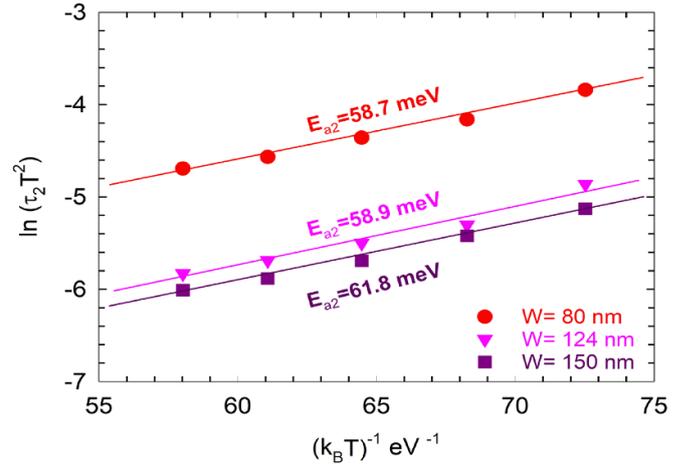


Figure 8. Modified Arrhenius plot for the relaxation times at the higher temperatures ($T > 150$ K) in SSDs with different widths. The symbols correspond to the values of τ_2 obtained, by means of equation (4), from the experimental τ_{peak} and the values of τ_1 obtained from the fittings to equation (3). The lines are the fittings of the data so obtained to equation (5).

From the experimental values of τ_{peak} and the values of τ_1 obtained from the fittings to equation (3), it is possible to estimate τ_2 at each temperature in every device. The values of τ_2 so obtained for high temperatures ($T > 150$ K) are shown for the three device widths in figure 8, together with their Arrhenius fitting. τ_2 , unlike τ_1 , obeys the dependence typical of bulk traps, like those found in AlGaIn/GaN HEMTs [9, 10],

$$\tau_2 T^2 = k_{02} \cdot \exp\left(\frac{E_{a2}}{k_B T}\right), \quad (5)$$

where k_{02} is a pre-exponential factor independent of temperature, from which the capture cross section of the traps can be determined. From the fittings, the activation energy in each of the three SSDs under analysis has been obtained (shown in figure 8). The values are quite similar (≈ 60 meV), what strongly suggests that they are caused by the same bulk trap. Indeed, several works have found bulk traps with analogous activation energies in AlGaIn/GaN HEMTs [10, 37]. For completeness, in figure 6 we have plotted with blue lines the values of τ_2 obtained from the fittings to equation (5), and with dashed black lines the values of τ_{peak} resulting from equation (4), combining the values of τ_1 and τ_2 obtained from their respective fittings. As observed, the agreement found with the experimental data is quite satisfactory in the three SSDs under analysis, what supports our interpretation of the results.

4. Conclusions

We have studied the performance of GaN-based SSDs as zero-bias RF detectors in a wide range of temperatures. A diode with channel length $L = 1 \mu\text{m}$ and width $W = 80$ nm was analyzed, showing a significant increase of the responsivity at low temperatures accompanied by a drop-off in frequency, what suggests the existence of traps. To understand this behavior,

DC and AC characterizations were made. DC measurements showed a decrease of the zero-bias resistance with the increase of temperature, which is attributed to the thermal activation of traps located at the sidewalls of the channel. Additionally, a fairly good agreement was found between the RF results and the values calculated within a quasi-static model based only on the DC I - V curves. AC small-signal impedance measurements were also performed, and proved to be an effective tool to characterize the traps, giving evidence of a double origin (surface and bulk) of the traps in the SSDs. Charge captured at the surface traps is responsible for the anomalous behavior found at low temperatures both in the responsivity and the resistance of the diodes. Surface traps were found to exhibit a behavior typical of a relaxation process characterized by a spread of times, as expected from the distributed energy levels within the gap originated by the etching of the channel. The analysis of SSDs with different channel widths confirmed that the surface effects related to traps found at low temperatures are more relevant the narrower is the channel.

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